An Architecture for Resilient Federated Learning through Parallel Recognition

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Abstract

Federated learning allows collaboration of multiple intelligent devices without affecting each other [1]. In this paper, we propose an architecture for resilient federated learning employing triplication of AI processors with different intelligence. The proposed architecture performs parallel recognition with lightweight algorithm and improves accuracy through federation. Experimental results show that the improved accuracy is 2.3% above compared to accuracy of a single AI processor on average and guarantees resilience.

Architecture

The proposed architecture includes the parallelized AI processors and an arbiter. The AI processors utilize devised protocol for learning and recognition process. The protocol contains 4 parts as follows:

- **Processor Selection**: Active condition of the processors for each bit
- **Mode Setup**: 3bits for mode (read/write, single data/consecutive data) selection and 5bits for address
- **Data Length and elements**: Data for Learning/Recognition process
- **Category**: Category for Learning process

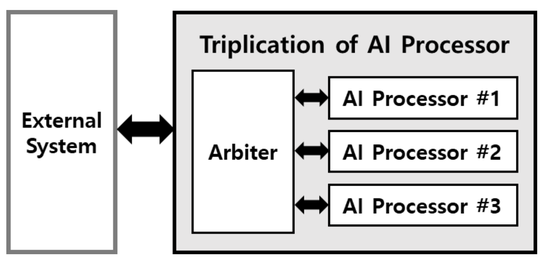


Figure 1. Triplication of AI Processor

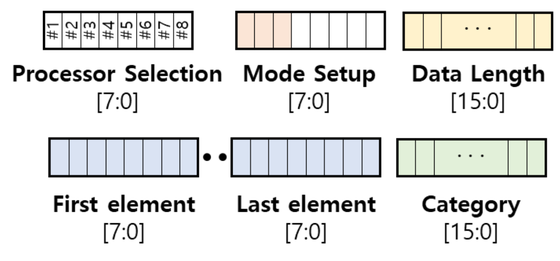


Figure 2. Protocol for Proposed Architecture

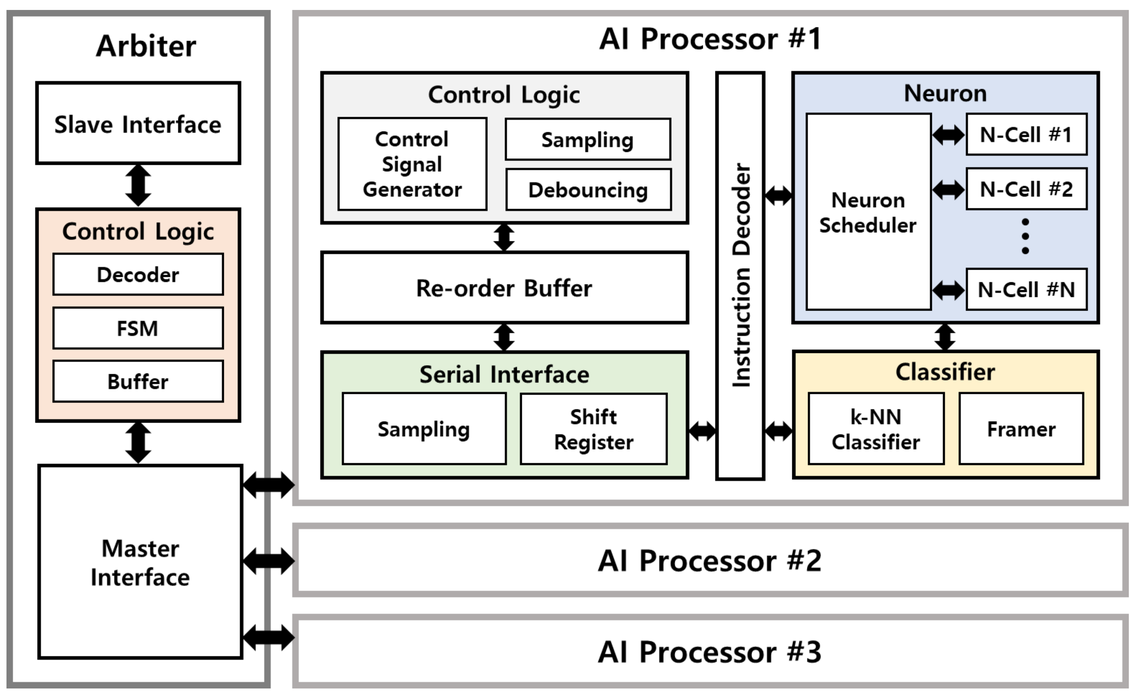


Figure 3. The Proposed Architecture for Resilient Federated Learning

✓ AI Processor

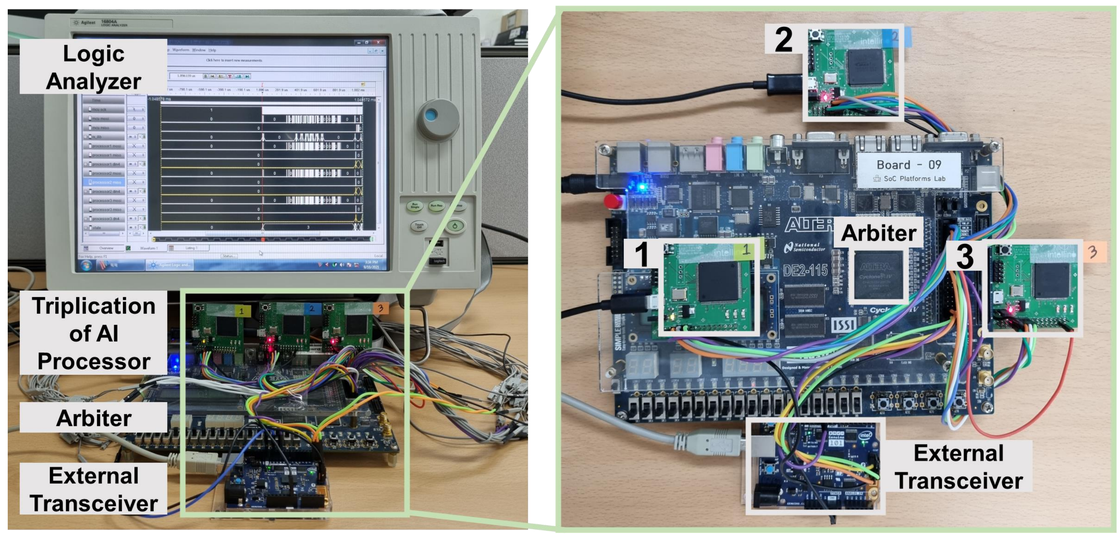
- **Different intelligence**: 1) With different learning data
  2) Through reconfiguration
- **Lightweight**: Applying Manhattan distance-based k-NN algorithm enables multiplication units unnecessary.

✓ Arbiter

- **Parallel recognition**: Obtain recognition results simultaneously from the AI processors.
- **Aggregation**: Determine final recognition output by a majority vote and a weight parameter.

Implementation

- **Covering fault result**: Implementation of triplication architecture enables a majority vote as shown in Fig. 5.
- **Improving accuracy**: The accuracy was verified by the simulator from [2]. The AI processors cooperate each other and the improved accuracy is 2.3% above compared to single AI processor as shown in Fig. 6.
- **Low-power consumption**: The power consumption of the AI processor during learning and recognition process was under 800mW.



- Cyclone IV FPGA: The Arbiter
- Max10 FPGA: The AI Processors

Figure 4. Experimental Environment

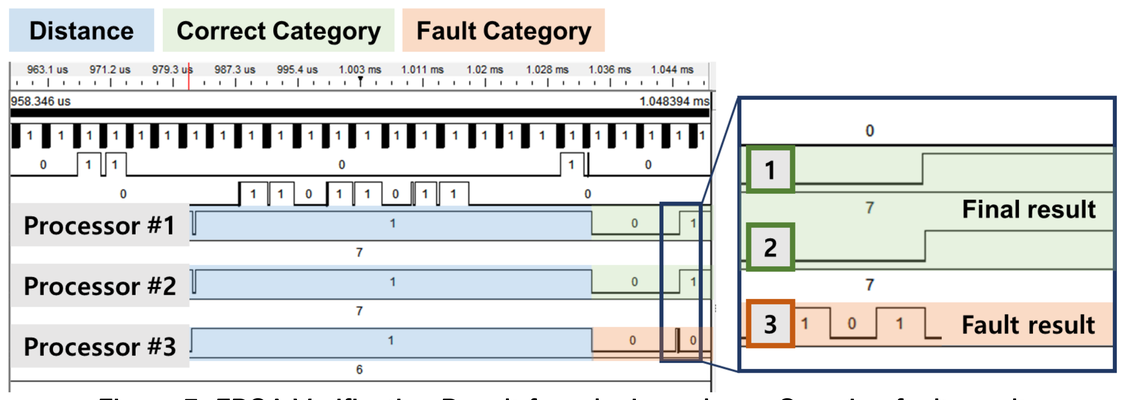


Figure 5. FPGA Verification Result from logic analyzer: Covering fault result

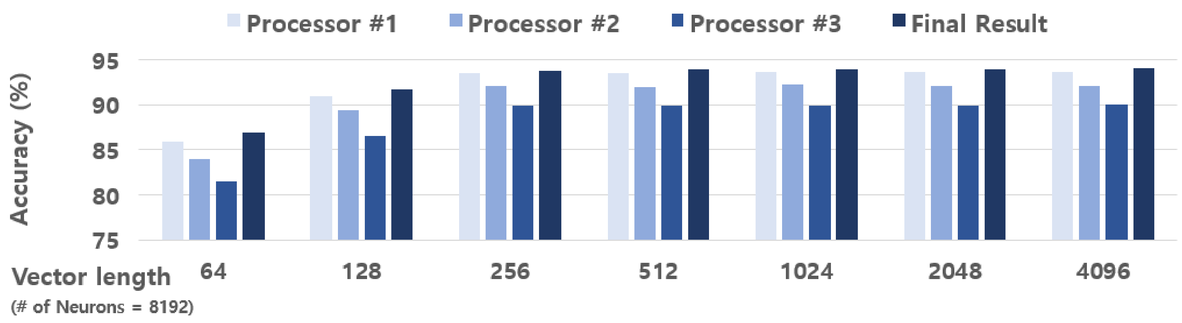


Figure 6. Accuracy of the Proposed Architecture: Improving accuracy

Conclusion

- The proposed architecture supports resilient federated learning through parallel recognition.
- The proposed architecture improves accuracy by federation and mask fault result.

Acknowledgement

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[1] Alessandro Giuseppi et al. "AdaFed: Performance-based Adaptive Federated Learning," International Conference on Advances in Artificial Intelligence (ICAAI), 2021, pp. 38–43.
[2] Hwang, D.H, Han, C.Y, Oh, H.W, Lee, S.E, "ASimOV: A Framework for Simulation and Optimization of an Embedded AI Accelerator," Micromachines, Vol. 12, No. 838, July. 2021.